



A 3-D Microcomputer Module Study

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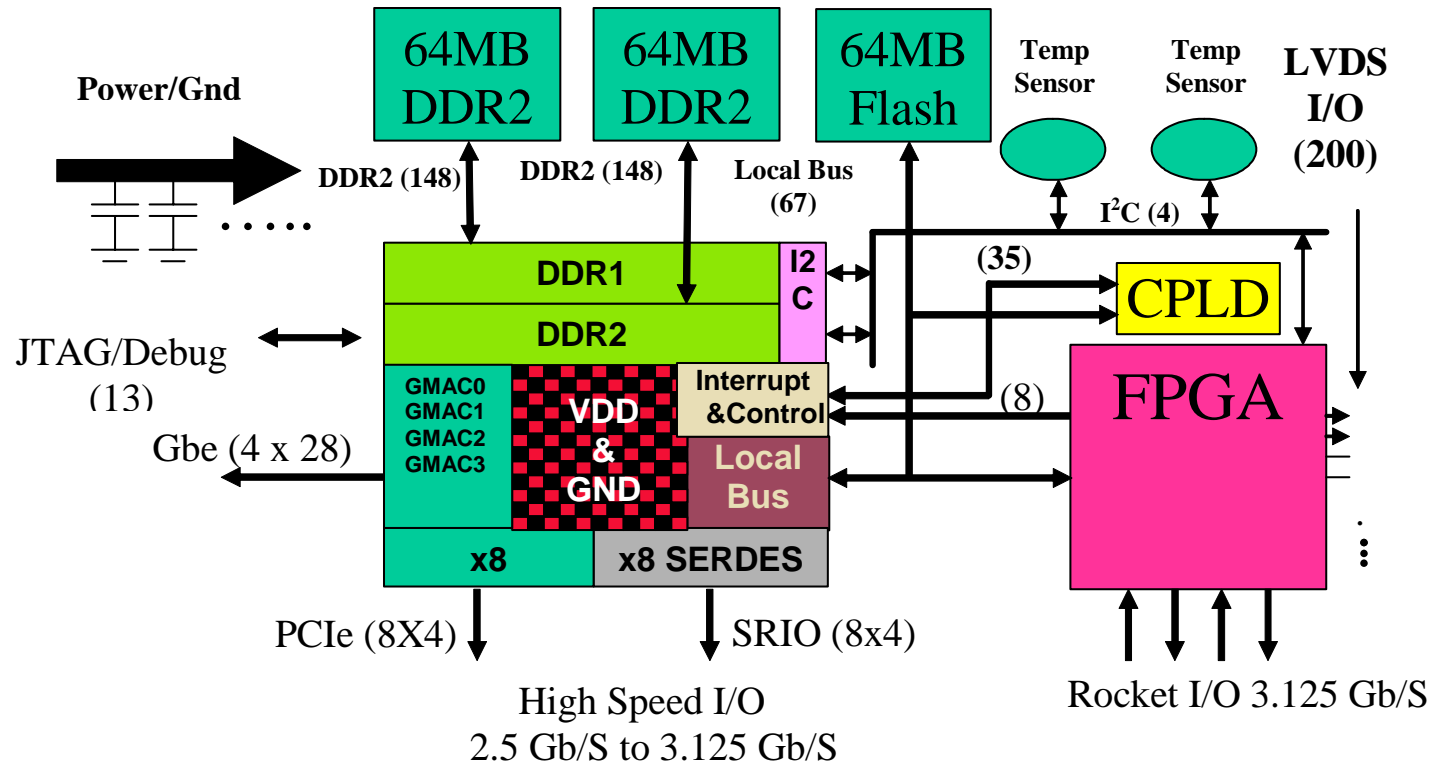
Trends in Military/Space Electronics

- High functional performance/COTS
- Small form factor
- Low cost/COTS
- Conduction cooling
- High reliability
 - Vibration
 - Shock
 - Thermal Cycling

Function of 3-D Computer in Missile Application

- Accepts digitized spectral information from the missile sensors.
- Processes digital information to discriminate “target” from “non-targets”.
- Generates digital target profile.
- Target information is used for missile guidance and payload control.
- Several computer modules proposed for use in a single missile.

Microcomputer Block Diagram



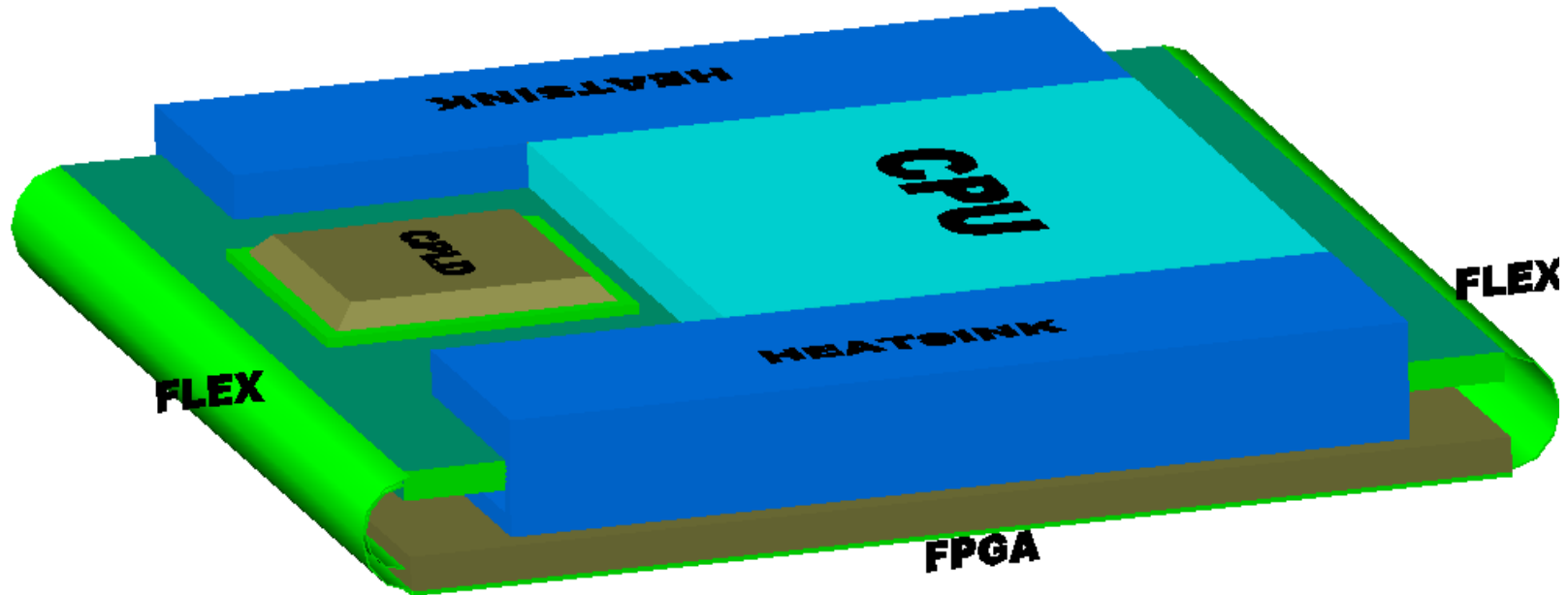
Application Requirements/Specifications

- Size: 2.4 “ x 2.4” x .35”
- Weight:.2 LBS
- ~1080 ball outs
- Conduction Top Plate
- Dual Core 8641D CPU Up to 1.5 GHz w/Altiavek
- 466 MHz DDR2 SDRAM Up to 1 GB
- Dual Core version has 2 DDR2 Interfaces 64MB to 512MB
- 4X 2.5 GHz PCI Express (PCIe) Interfaces
- 4X 3.125 GHz Serial Rapid IO (SRIO) Interfaces
- 4X GBE Interfaces
- Up to 512 MB (NAND) Flash Boot Memory
- FPGA based Quad 3.125 GHz Rocket I/O Interfaces
- Two Local Bus Interfaces to CPLD and FPGA
- Dual DS 1772 Thermal Sensors

Package Design Features

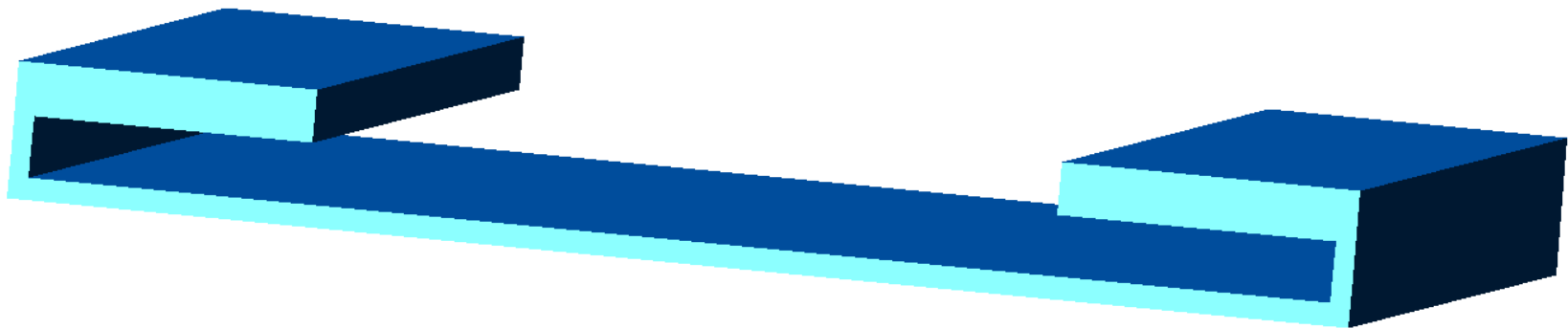
- Novel Heat Sink Design
- Stacked Components- Tessera uZ-technology
- Rigid Flex Folded Substrate
- Embedded Passives
- Low Profile Components

3-D Microcomputer Package Assembly



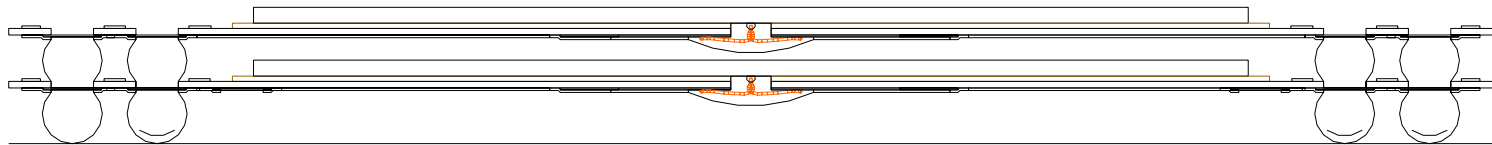
Novel Heatsink Design

- Wraps around the upper substrate to conduct heat from the top of FPGA to the coldplate.
- Current design material is nickel-plated copper.
- Implementation requires rather unique assembly techniques.

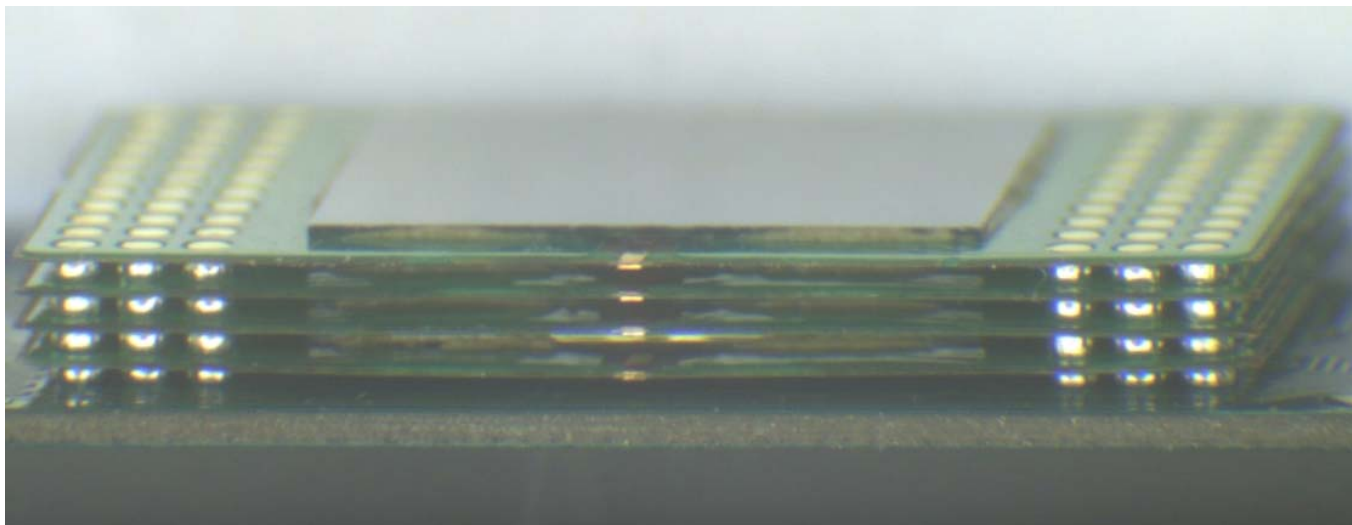


NxGEN μ Z-ball Stacks

- Die are attached to a flex substrate using a compliant adhesive.
- DRAM bond pads are wirebonded through the slot up to the substrate bond pads.
- The wirebonds are encapsulated and solder balls are then reflowed onto the solder pads.
- Individual layers are then stacked to form a completed 3-D package.

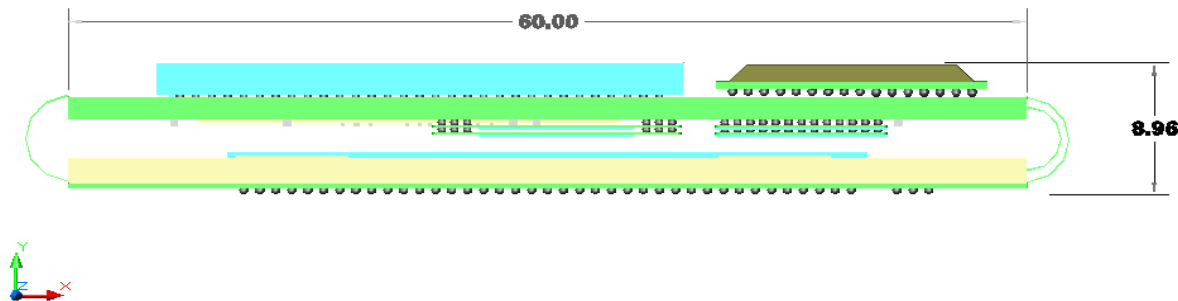


NxGEN μ Z-ball Stacks



Rigid Flex PCB

- Up to 16 layers might be required for rigid sections.
- Illustration shows two flex connections on the right and a single one on the left.
- Up to 4 flex connections are possible.
- The connection on the left is done using an anisotropic adhesive attachment or soldering operation. Multiple connections are also possible.
- The maximum allowable flex connections for sufficient signal and power ground plane integrity.



Low Profile Components

- 0201 Resistors and Capacitors are readily available with 1005 components now becoming available.
- Low frequency bypass capacitors tend to have a large footprint as well as being high-profile.
- More recent capacitors are available with fairly high capacitances, (47ufd) and low profile ~.4 mm.



Buried Components

- Ohmega-Ply Resistors can be used for buried resistors.
 - Best used for a tight range of values.
 - Difficult to get un-trimmed tight tolerances.
 - Need different layers for different ranges of resistances.
- Buried cores of high dielectric materials in substrate can be used for high-frequency bypass capacitors
 - DuPont HK BC Material

Rigid Flex PCB

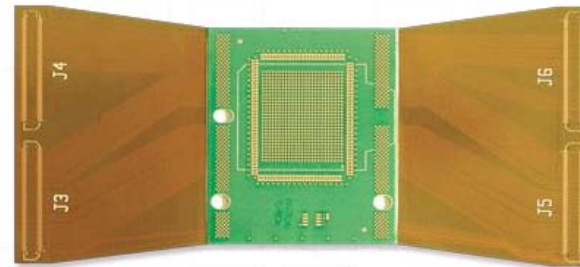
RIGID FLEX

HIGH LAYER COUNT • HIGH SPEED • HDI

Silicon Testing

Specifications

Layers: 14 rigid; 3 flex
Material: High Speed FR4 (Isola 408)
Dupont AP Flex material
Trace Width: 0.002" ± 0.0003"
Controlled Impedance (64 ohms ± 10%)
Buried resistors (400 each of Ohmega
60 ohm ± 10%)
Buried capacitors (900 each)
Surface Finish: Entek 106



[Download PDF of Rigid Flex](#)
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Thermal Analysis : Assumptions

- From the 3-D model a FEM thermal analysis was conducted using SolidWorks COSMOS. The following power assumptions were made for the various components

COMPONENT	POWER (W)
CPU	20
FPGA	10
DRAM DIE	1 (8 TOTAL)
FLASH DIE	0

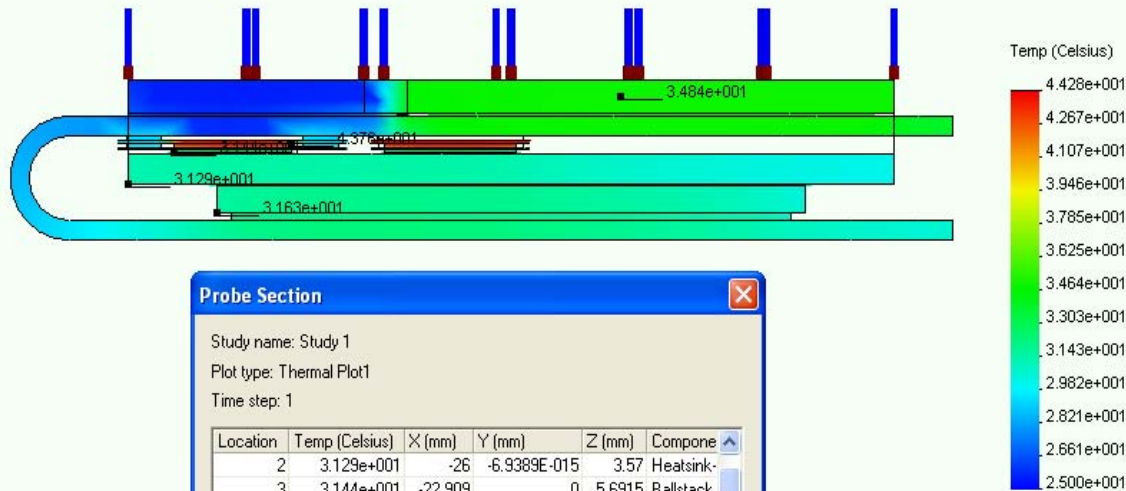
Table 1. Component Power Dissipations

Thermal Analysis Assumptions

- Coldplate set at 25°C and assumed it is in direct contact with the FPGA die.
- Maximum junction temperature is assumed to be 115° C.
- Given a maximum cold plate temperature of 85 °C. then the maximum allowable delta between junction and the cold plate will be 30 °C.
- Stacks were modeled with a thermally conductive material bonding the layers together.

Module Thermal Requirements

Model name: Package Assembly
Study name: Study 1
Plot type: Thermal Plot1
Time step: 1



Probe Section

Study name: Study 1
Plot type: Thermal Plot1
Time step: 1

Location	Temp (Celsius)	X (mm)	Y (mm)	Z (mm)	Compon
2	3.129e+001	-26	-6.9389E-015	3.57	Heatsink-
3	3.144e+001	-22.909	0	5.6915	Ballstack
4	4.376e+001	-14.949	0	6.2633	Ballstack
5	3.484e+001	7.4787	0	9.2856	CPU - an

Clear Save Plot Response
Close Help

Thermal Analysis Results

- Results from the thermal analysis indicates temp rise 6 °C for FPGA. An actual temperature rise over 10 °C would not be expected.
- The lower DRAM die on the stack packages runs the hottest with a cold-plate-to-junction temperature of 20 °C.

Summary

- Demonstrated feasibility of a multiple technique approach for a 3-D micro-computer module.
- Further work will involve substrate layout analysis, electrical analysis and prototype development.