



# A 3-D Computer Module Study

**Don Hayashigawa**  
**NxGEN Electronics, Inc.**

9771 Clairemont Mesa Blvd., San Diego, CA 92124  
www.NxGENelectronics.com donh@NxGENelectronics.com +1 (858) 309-6610, x3014

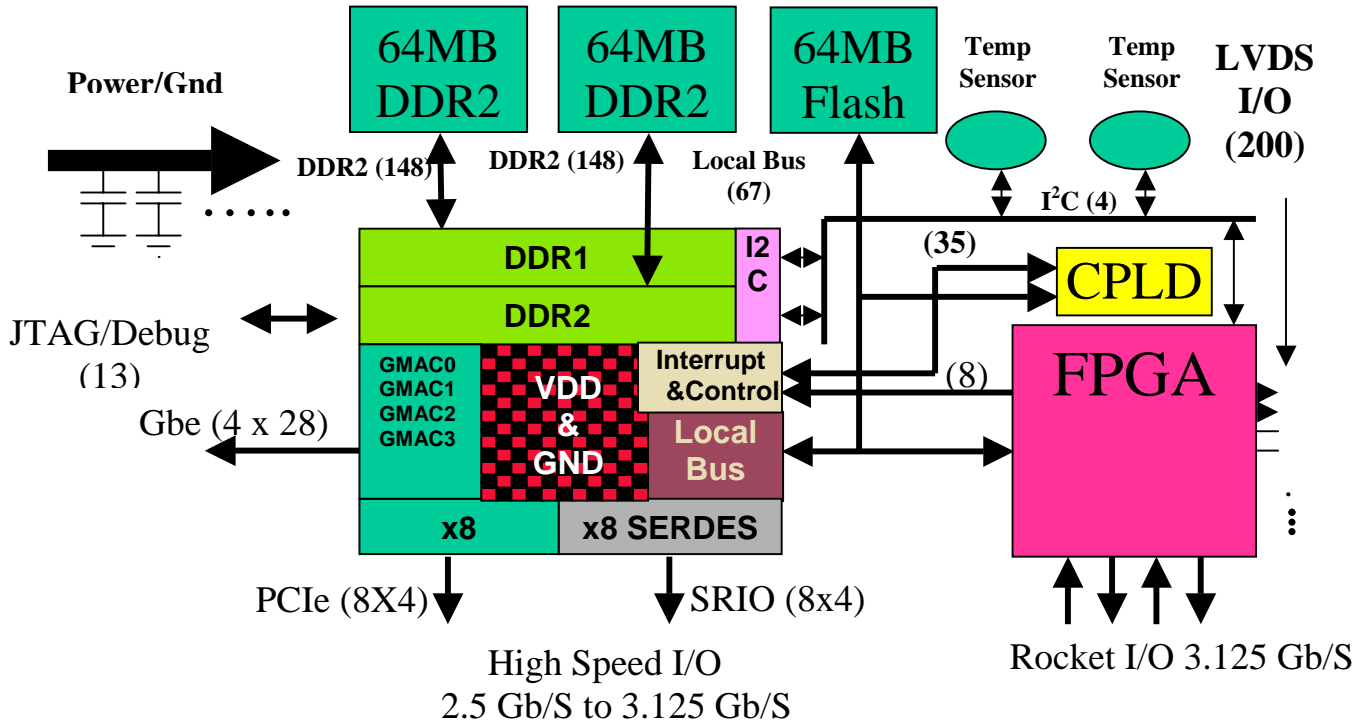
## **ABSTRACT**

This paper outlines a study for the development of a small form-factor 3D-Microcomputer Module for a military application, based on COTS devices. The process, from establishing the module functional requirements to the development and analysis of a preliminary package design, will be examined. The main discussion will center on how the mechanical, electrical and thermal requirements can be met by adopting different packaging strategies, including CSP stacking, rigid-flex PCB, embedded passives, low profile components and a novel heat sink design. Finally, the results of the analyses done to validate this system-in-package design will be presented.

## **INTRODUCTION**

The current trend in military space electronics is to utilize the latest COTS (Commercial-Of-The-Shelf) technology in such a way that they can still meet the demanding requirements of the target application, including low cost, small form factor, conduction cooling, high reliability and functional performance. A major building block in a missile application is the microcomputer, whose “main purpose to accept the digitized spectral information from the sensors, process the information so that the ‘target’ can be discriminated from ‘non-targets’ and generate signals for the missile control and payload systems to turn towards the target...”<sup>1</sup>. The subject of this paper is the development of the preliminary package design for a 3-D microcomputer module intended for this purpose.

The preliminary requirements and specifications for the module were determined with the customer. A block diagram was initially generated and subsequently modified by the customer, as shown in figure 1 below.



**Figure 1. Block Diagram**

The key features required to meet the computing and communications requirements and specifications of the target application include the following:

- Size: 2.4 “ x 2.4” x .35”
- Weight: .2 LBS
- ~1080 ball outs
- Dual Core 8641D CPU Up to 1.5 GHz w/Altiavek
- 466 MHz DDR2 SDRAM Up to 1 GB
- Dual Core version has 2 DDR Interfaces 64MB to 512MB
- 4X 2.5 GHz PCI Express (PCIe) Interfaces
- 4X 3.125 GHz Serial Rapid IO (SRIO) Interfaces
- 4X GBE Interfaces
- Up to 512 MB (NAND) Flash Boot Memory
- FPGA based Quad 3.125 GHz Rocket I/O Interfaces
- Two Local Bus Interfaces to CPLD and FPGA
- Dual DS 1772 Thermal Sensors

Some of the environmental requirements include the following:

- Operating Temperature Range: -40 to +85°C
- Non-operating Temperature Range: -55 to +105°C
- Vibration: VITA 47 Level V3
- Shock: 40g, 11 millisecond half-sine

## PACKAGE DESIGN

The package design developed for the above requirements is depicted in the 3-dimensional view of figures 3. and the side view of figure 4. Standard packaging for the CPU and the FPGA was selected due to the high cost and unavailability of fully tested bare die. In order to maintain the footprint size, it was necessary that the CPU and the FPGA be in some way mounted one over the other. One method for doing so is through the use of a flex substrate on which the FPGA and CPU are mounted on separate rigid substrates. Because the CPU dissipates the most power, it was located on the upper substrate in direct contact with the coldplate, while the FPGA was mounted below. For reasons of minimizing real estate and minimizing trace lengths, the CPLD and memory were placed on the same rigid substrate as the CPU. The CPLD is again assumed to be a COTS packaged device and placed on top, while the flash and DRAM are located on the opposite side of the CPU. The package I/O are implemented as an array of solder balls on 1 mm pitch.

One unique feature of this package is the folded copper heatsink which wraps around the upper substrate and is used to conduct heat from the top surface of the FPGA to the coldplate. In many military space applications, there is no available airflow and the motherboard is usually running at a fairly-elevated temperature, so the coldplate was assumed to be the only source for cooling of the module.

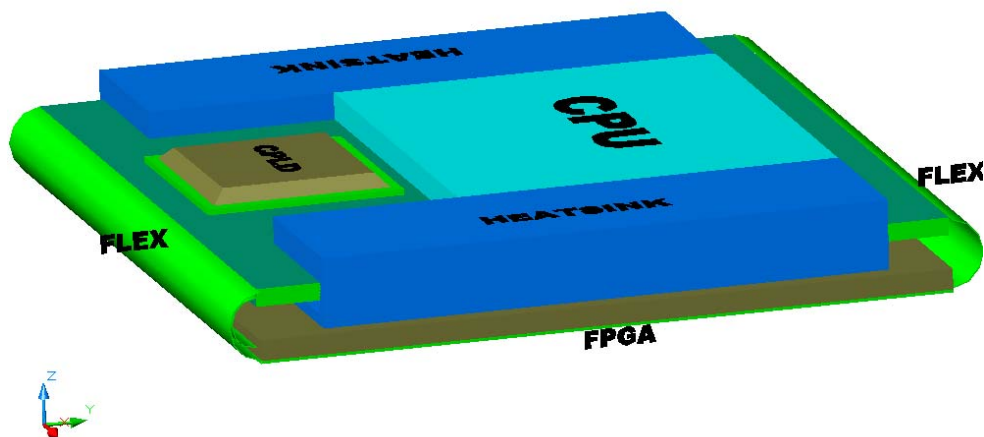
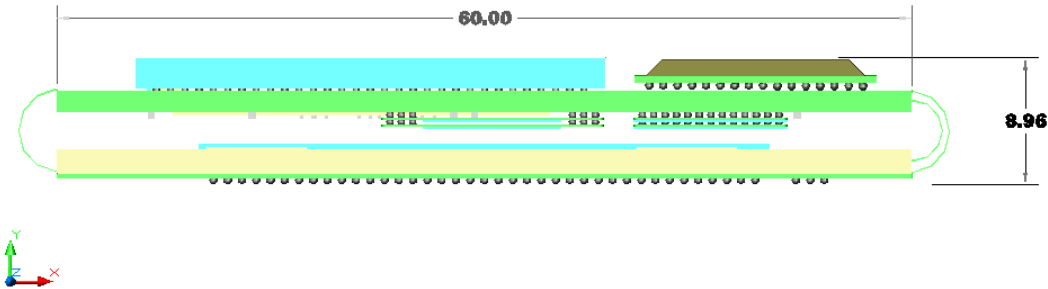


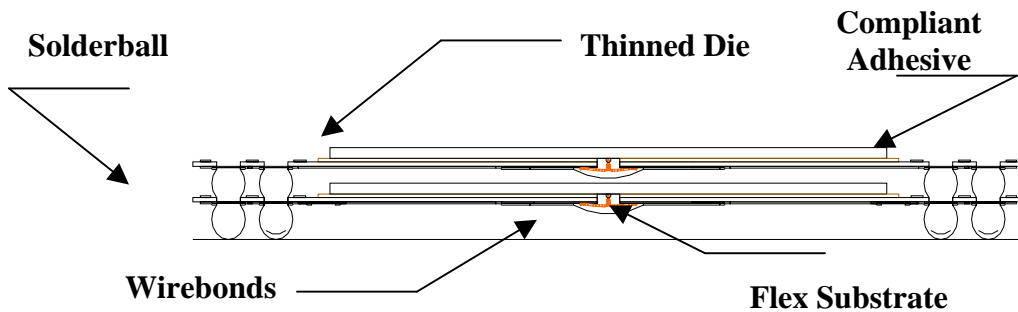
Figure 3. Model of 3-D Microcomputer Module



**Figure 4. Side View of Model of 3-D Microcomputer Module  
 (Heat sink removed for visibility)**

The side view of figure 4 shows the DRAM and flash memory implemented as Tessera  $\mu$ Z-ball Stacks™. A more detailed view of such a stack with its basic construction is shown in figure 5. In this technology, wafers are obtained from various DRAM manufacturers and thinned down from 150 microns to as low as 75 microns. The die are then placed face down and attached to a flex substrate using a compliant adhesive. The compliant adhesive acts to mechanically decouple the low-CTE die from the higher-CTE PCB on which the stack is mounted and provides inherent reliability to the stack.

The substrate has a slot running down the middle of it, which reveals the center row of bond pads of the attached DRAM die. The assembly is then flipped over and DRAM bond pads are wirebonded through the slot up to the substrate bond pads. The bond pads are then connected via traces to rows of solder balls pads on each side of the substrate. The wirebonds are encapsulated and solder balls are then reflowed onto the solder pads. The layers can then be stacked and reflowed to create the final assembly.



**Figure 5 . Detailed View of 2-Layer  $\mu$ Z-ball Stack™**

Wafer probed memory die are becoming available through manufacturers such as Micron, Samsung and others. In addition, each stack layer can be further tested as an individual CSP prior to final assembly. This greatly enhances the overall yield of the stack. Thus, although not strictly COTS, memory stacks are inherently cost-effective, reliable and small-form factor components, which are ideally suited for applications such as this.

With regard to the rigid-flex substrate, it is assumed that there may be as many as 16 layers might be required. The side view in figure 4, shows flex connections on either side of the substrate. On the right side, two flex cables are shown connecting the upper and lower sections, but up to 4 is possible. The maximum allowable number of flex connections between rigid sections is critical to assuring not only sufficient signal interconnect, but also power ground plane integrity. On the left side of figure 4 is another flex connection, which would be achieved after the assembly is folded. This connection could be achieved through a spot soldering operation or an ACA (anisotropic conductive adhesive) attachment.

There are clearly many passive components which would be required for a functional microcomputer including high-frequency and low-frequency bypass capacitors, bias and termination resistors and frequency control capacitors. Termination resistors can be embedded into the substrate using Ohmega-Ply™ resistors, while high-frequency bypass capacitance can be achieved through buried capacitive layers. Low frequency bypass capacitors tend to have a large footprint as well as being high-profile. However, some capacitors have recently become available which have fairly high capacitances (10ufd) and low profile ~.5 mm.

Another key requirement is the shock and vibration requirements. The component as designed does appear to meet the weight specifications, however, to meet the vibration and shock requirements, it appears that some form of mechanical restraint would be required. The simplest approach would be to bolt the heatsink to the PCB through holes drilled in the heatsink.

## THERMAL ANALYSIS

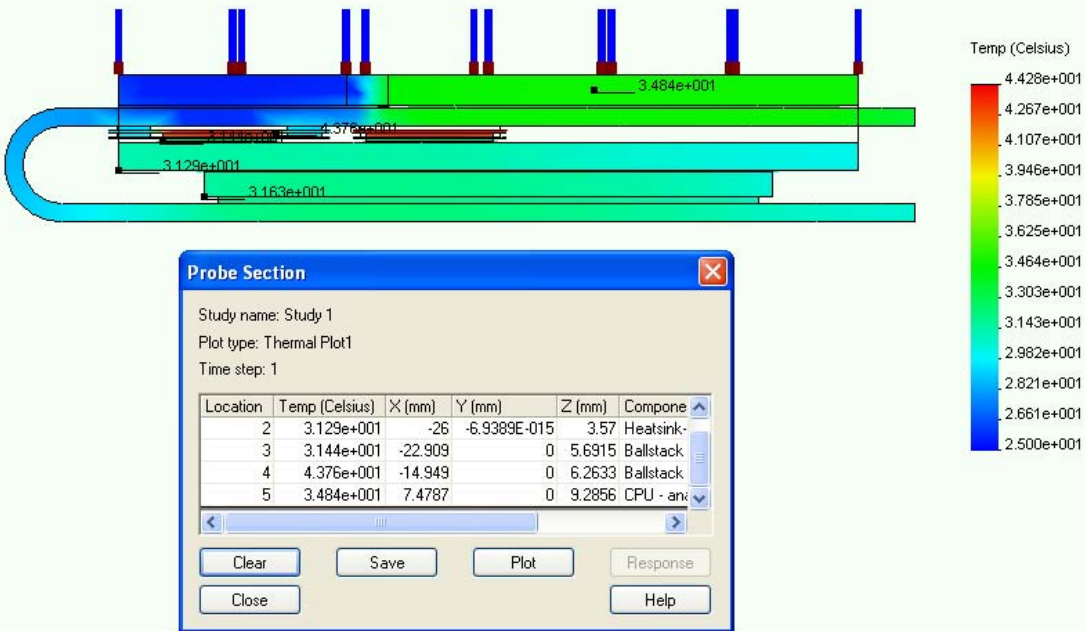
From the 3-D model a FEM thermal analysis was conducted using SolidWorks COSMOS. The following power assumptions were made for the various components.

COMPONENT	POWER (W)
CPU	20
FPGA	10
DRAM DIE	1 (8 TOTAL)
FLASH DIE	0

**Table 1. Component Power Dissipations**

The cold plate was set arbitrarily at 25°C and it was assumed that it was in direct contact with the FPGA die. If the maximum junction temperature is assumed to be 115 °C, then the maximum allowable delta between junction and the cold plate would be 30 °C, given the maximum cold plate temperature of 85 °C. The results from the thermal analysis indicates a temperature of rise of 6 °C, which is probably a little overly optimistic as the die was assumed to be the same size as the FPGA package. Still, a temperature rise over 10 °C would not be expected. The lower DRAM die on the stack packages runs the hottest with a cold-plate-to-junction temperature of 20 °C. It should be noted that the stacks were modeled with a thermally conductive material bonding the stacks together. The assumptions for the DRAM die dissipation were given by the customer, however, it is likely that the DDR2 die will run significantly cooler.

Model name: Package Assembly  
 Study name: Study 1  
 Plot type: Thermal Plot1  
 Time step: 1



## CONCLUSION

A preliminary package design for a 3D microcomputer module targeted for a demanding military space application was completed. This design incorporates a novel heatsink design, a rigid-flex substrate, buried /low profile passive components and uZ-ball stack™ components. A simplified thermal analysis indicates that the module should meet the thermal requirements. To the extent possible, it appears that all the other specifications and requirements for this device are being met.

The other tasks required to complete the development include: rad- hard design, complete layout and electrical analysis, preliminary layout, final analyses, final design and development of a functional prototype.



## REFERENCES

1. R. Czajkowski, SBIR Final Report (Contract HQ0006-05-C7-190), "3D Computer Module, NxGEN Electronics Inc.", 2006.
2. Vern Solberg, Ignacio Osorio, and Jeffrey Demmin Tessera, "BALL STACK PACKAGING FOR HIGH PERFORMANCE MEMORY", Tessera Inc., SMTA International, September, 2003.